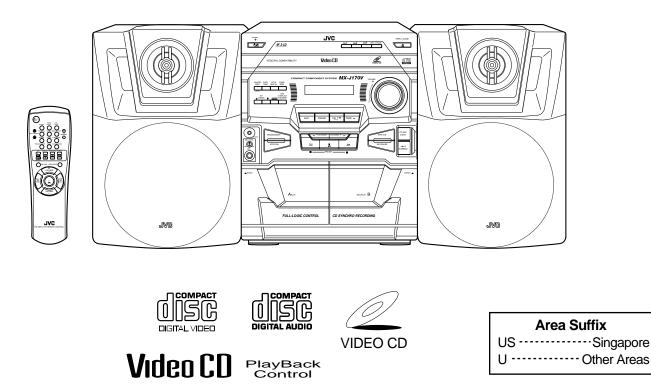


JVC SERVICE MANUAL

COMPACT COMPONENT SYSTEM

MX-J170V



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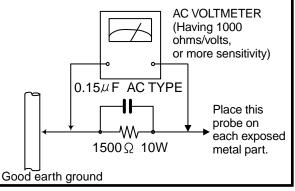
-Safety Precautions-

- 1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
- 2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer's warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
- 3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (<u>()</u>) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
- 4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
- 5. Leakage current check (Electrical shock hazard testing) After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock. Do not use a line isolation transformer during this check.
 - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.)
 - Alternate check method

Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having 1,000 ohms per volt or more sensitivity in the following manner. Connect a $1,500\Omega$ 10W resistor paralleled by

a 0.15μ F AC-type capacitor between an exposed metal part and a known good earth ground. Measure the AC voltage across the resistor with the AC voltmeter. Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and measure the AC

voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. Voltage measured any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



-Warning

- 1. This equipment has been designed and manufactured to meet international safety standards.
- 2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained. 3. Repairs must be made in accordance with the relevant safety standards.
- 4. It is essential that safety critical components are replaced by approved parts.
- 5. If mains voltage selector is provided, check setting for local voltage.

CAUTION Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

Important for laser products

1.CLASS 1 LASER PRODUCT

- **2.DANGER :** Invisible laser radiation when open and inter lock failed or defeated. Avoid direct exposure to beam.
- **3.CAUTION :** There are no serviceable parts inside the Laser Unit. Do not disassemble the Laser Unit. Replace the complete Laser Unit if it malfunctions.
- **4.CAUTION :** The compact disc player uses invisible laserradiation and is equipped with safety switches whichprevent emission of radiation when the drawer is open and the safety interlocks have failed or are de feated. It is dangerous to defeat the safety switches.
- **5.CAUTION :** If safety switches malfunction, the laser is able to function.
- **6.CAUTION :** Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

▲ CAUTION Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.

- VARNING : Osynlig laserstrålning är denna del är öppnad och spårren är urkopplad. Betrakta ej strålen.
- VARO : Avattaessa ja suojalukitus ohitettaessa olet alttiina näkymättömälle lasersäteilylle.Älä katso säteeseen.

ADVARSEL : Usynlig laserstråling ved åbning , når					
sikkerhedsafbrydere er ude af funktion. Undgå					
udsættelse for stråling.					
ADVARSEL : Usynlig laserstråling ved åpning,når					
sikkerhetsbryteren er avslott. unngå utsettelse					
for stråling.					

REPRODUCTION AND POSITION OF LABELS								
	WARNING LABEL							
	DANGER : Invisible laser radiation when open and interlock or defeated. AVOID DIRECT EXPOSURE TO BEAM (e)	VARO : Avattaessa ja suojalukitus ohitettaessa olet alttiina näkymättömälle lasersäteilylle.Älä katso säteeseen. (d)	VARNING : Osynlig laserstrålning är denna del är öppnad och spårren är urkopplad. Betrakta ej strålen. (s)	ADVARSEL :Usynlig laserstråling ved åbning , når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling. (f)				
CLASS 1 LASER PROD								

Preventing static electricity

1. Grounding to prevent damage by static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

2. About the earth processing for the destruction prevention by static electricity

In the equipment which uses optical pick-up (laser diode), optical pick-up is destroyed by the static electricity of the work environment.

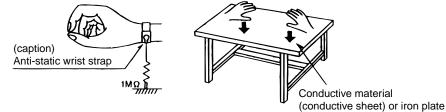
Be careful to use proper grounding in the area where repairs are being performed.

2-1 Ground the workbench

Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

2-2 Ground yourself

Use an anti-static wrist strap to release any static electricity built up in your body.



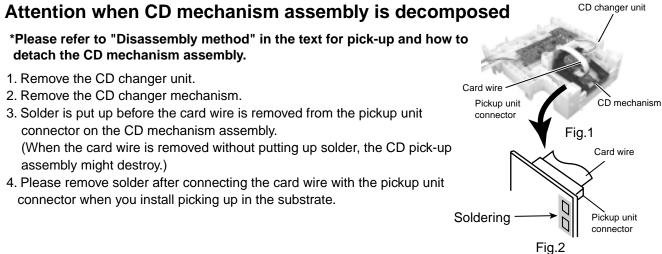
3. Handling the optical pickup

- 1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)
- 2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

4. Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.

- 2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.
- 3. Handle the flexible cable carefully as it may break when subjected to strong force.
- 4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it



В

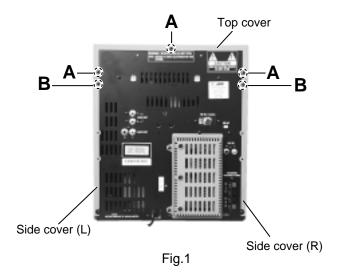
Disassembly method

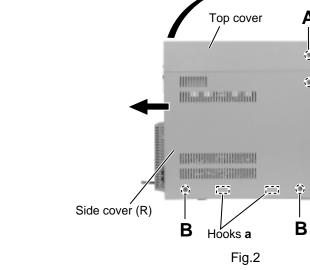
<Main body>

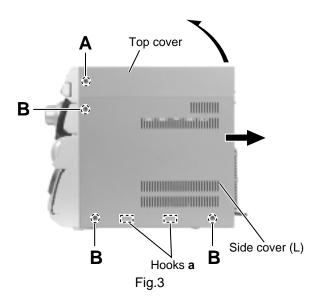
■ Removing the top cover and the side covers (See Fig.1 to 3)

- 1. Remove the five screws **A** on the back of the body and the both sides of the body.
- 2. Remove the top cover upward from behind.
- 3. Remove the eight screws **B** attaching the side covers on the back of the body and the both side of the body.
- 4. Slide the right and left covers backward and unhook the two hooks **a** in the lower part of the side covers as shown in Fig.2-2.

Hook







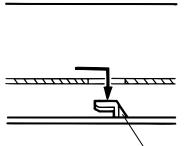


Fig.2-2 Hook

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Removing the CD Tray fitting (See Fig. 4 to 6)

- Prior to performing the following procedure, remove the top cover and the side covers.
 - ATTENTION: Be sure to remove the CD tray fitting before removing the CD changer unit.
- 1. Press the POWER button. Press the OPEN/CLOSE button to eject the CD tray.
- 2. Move the CD tray fitting upward and release the joint **b**.
- 3. Press the OPEN/CLOSE button to insert the CD tray.

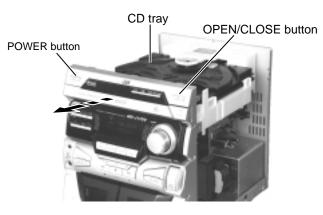


Fig.4

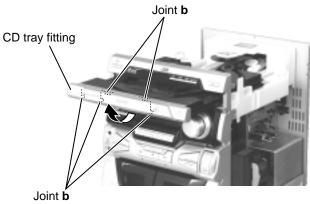


Fig.5

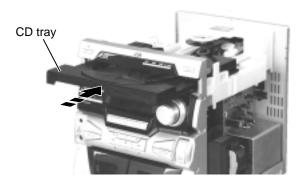


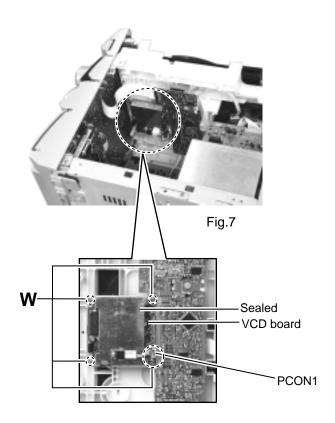
Fig.6

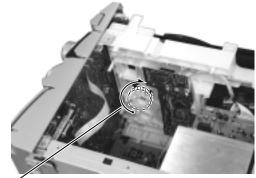
Removing the CD Tray fitting & the VCD board (See Fig.7 to 10)

- How to eject the CD tray without turning on power -
- Prior to performing the following procedure, remove the top cover and the side covers.

ATTENTION: Be sure to remove the CD tray fitting before removing the CD changer unit.

- 1. Disconnect the harness from connector PCON1 of the VCD board.
- 2. Remove the four screws ${\bf W}$ attaching the sealed and VCD board.
- 3. Turn the black loading pulley gear marked **c** from the back of the CD changer unit as shown in Fig.8 and draw the CD tray toward the front.
- 4. Move the CD tray fitting upward and release the joint **b**.
- 5. Push and insert the CD tray manually.





Marked **c** ______ Loading pulley gear

Fig.8

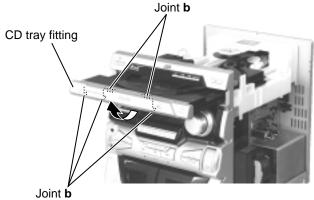
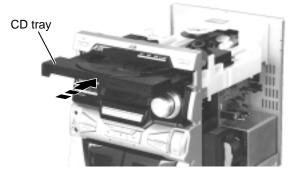


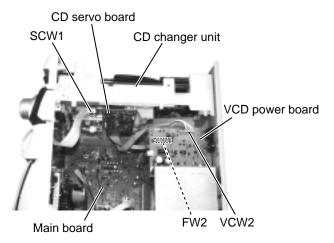
Fig.9



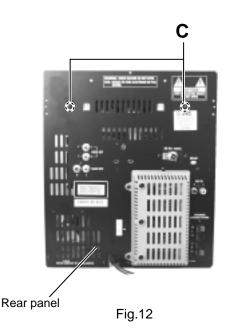
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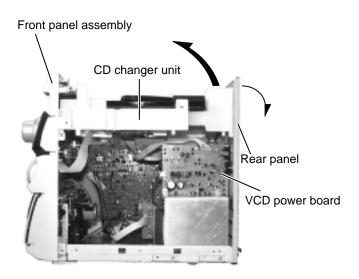
Removing the CD changer unit (See Fig.11 to 13)

- Prior to performing the following procedure, remove the top cover, the side covers and the CD Tray fitting.
- 1. Disconnect the card wire from connector SCW1 of the CD servo board on the back of the CD changer unit.
- 2. Disconnect the harness from connector FW2 on the inner side of the main board in the body.
- 3. Disconnect the harness from connector VCW2 on the VDC power board .
- 4. Remove the two screws **C** attaching the CD changer unit on the back of the body.
- 5. Draw the CD changer unit upward from behind while pulling the rear panel outward.











Removing the front panel assembly (See Fig.14 to 16)

- Prior to performing the following procedure, remove the top cover, the side covers, the CD Tray fitting and the CD changer unit.
- There is no need to remove the rear panel.
- 1. Disconnect the harness from head wire connector ECW1,DW1 and DW2 on the inner side of the main board in the body.
- 2. Disconnect the harness from connector HCW1 of the headphone board on the right side of the body.
- Remove the three screws D attaching the front panel assembly on both sides of the body.
 Remove the screw E attaching the earth terminal extending from the front compartment.
- 4. Remove the screw **F** attaching the front panel assembly on the bottom of the body.
- Release the two joints d on both sides and two joints e on the bottom of the body using a screwdriver. At the same time, disconnect the front compartment from connector CCW1 and CCW2 of the main board.

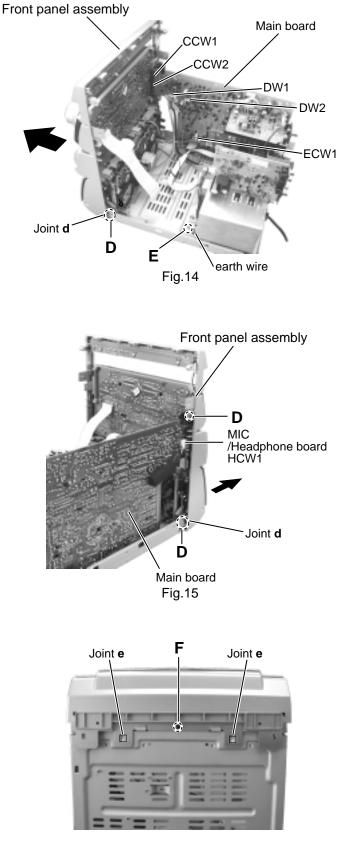
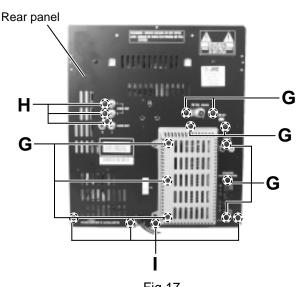


Fig.16

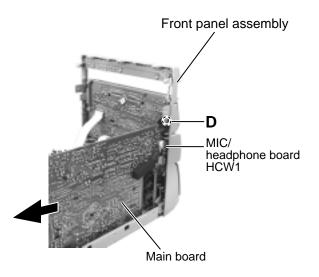
MX-J170V

■ Removing the rear panel (See Fig.17)

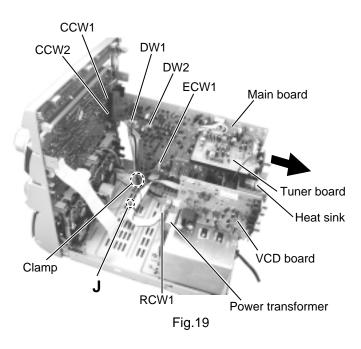
- Prior to performing the following procedure, remove the top cover, the side covers, the CD Tray fitting and the CD changer unit.
- There is no need to remove the front panel assembly.
- 1. Remove the ten screws **G** attaching the main board, the tuner board and the heat sink to the rear panel on the back of the body.
- 2. Remove the three screws **H** attaching the VCD power board to the rear panel on the back of the body.
- 3. Remove the four screws I attaching the rear panel on the back of the body.











Removing the main board (See Fig.18 and 19)

- Prior to performing the following procedure, remove the rear panel.
- 1. Disconnect the harness from connector HCW1 of the MIC/headphone board on the right side of the body. Release the harness from the clamp in the body.
- 2. Disconnect the harness from head wire connector ECW1,DW1 and DW2 extending to the main board in the body.
- 3. Disconnect the harness from connector RCW1 of the power transformer.
- 4. Remove the screws **D** attaching the front panel assembly on both sides of the body.
- 5. Remove the screw **J** attaching the earth terminal to the base chassis.
- 6. Disconnect connector CCW1 and CCW2 connected to the main board.

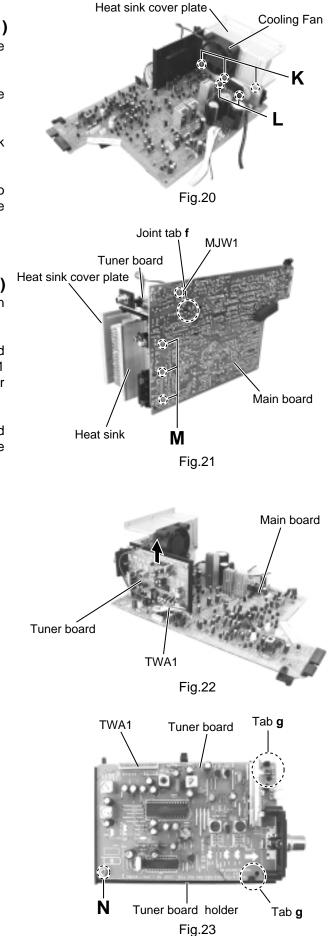
Removing the heat sink & cooling fan (See Fig.20 and 21)

- Prior to performing the following procedure, remove the main board.
- 1. Disconnect the harness from connector MJW1 of the main board.
- 2. Remove the three screws **K** attaching the heat sink cover plate and cooling fan.
- 3. Remove the two screws ${\bf L}$ attaching the power IC to the heat sink and the three screws ${\bf M}$ attaching the heat sink to the main board.

Removing the tuner Board

(See Fig.21 to 23)

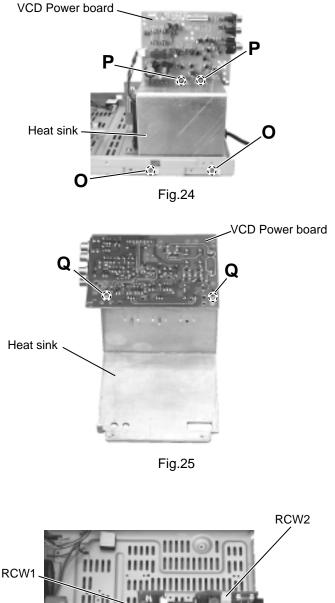
- The tuner board can be removed even if the main board is attached.
- Release the joint tab f of the tuner board holder and the main board, and disconnect connector FW1 connected to the main board. Remove the tuner board assembly (Refer to Fig.21).
- 2. Remove the screw **N** attaching the tuner board holder. Release the two tabs **g** outward and remove the tuner board from the tuner board holder.



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Removing the heat sink & VCD Power board (See Fig.24 and 25)

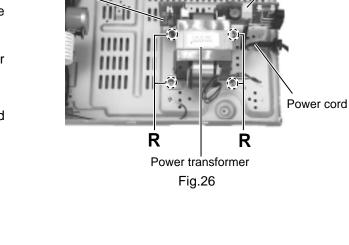
- Prior to performing the following procedure, remove the top cover and the side covers.
- 1. Remove the two screws **O** attaching the heat sink plate.
- 2. Remove the two screws **P** attaching the power IC to the heat sink and the two screws **Q** attaching the heat sink to the VCD Power board.



■ Removing the power transformer



- Prior to performing the following procedure, remove the VCD Power board.
- 1. Disconnect the power cord from connector RCW2 of the power transformer.
- 2. Disconnect the harness from connector RCW1 of the power transformer.
- 3. Remove the four screws ${\bf R}$ attaching the power transformer.
 - ATTENTION: Prior to disconnecting the power cord from the body, remove the rear panel.



<Front panel assembly>

• Prior to performing the following procedure, remove the top cover, the side covers, the CD tray fitting and the front panel assembly.

Removing the power / CD switch board (See Fig.27)

- 1. Remove the three screws **S** attaching the power/CD switch board and release the three tabs **h** outward.
- 2. Disconnect the harness from connector UCW9 of the power / CD switch board.

Removing the front board (See Fig.27 and 28)

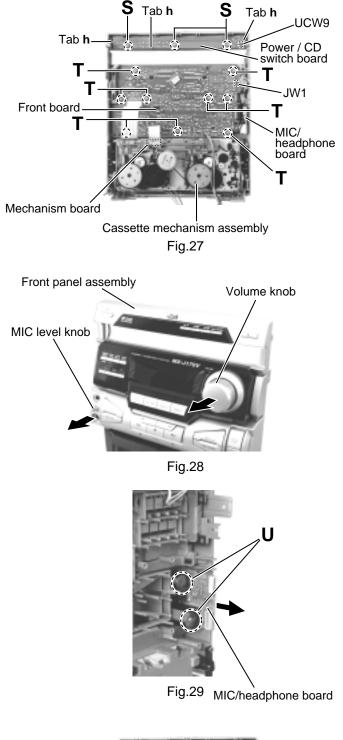
- Prior to performing the following procedure, remove the power / CD switch board.
- 1. Pull out the volume knob toward the front.
- 2. Disconnect the card wire from the mechanism board of the cassette mechanism assembly.
- 3. Remove the nine screws ${\bf T}$ attaching the front board.

Removing the MIC/headphone board (See Fig.28 and 29)

- Prior to performing the following procedure, remove the front board.
- 1. Pull out the MIC level knob toward you.
- 2. Remove the two screws **U** attaching the MIC/headphone board.

Removing the cassette mechanism assembly (See Fig.30)

- 1. Disconnect the card wire from the mechanism board of the cassette mechanism assembly.
- 2. Remove the seven screws ${\bf V}$ attaching the cassette mechanism assembly.



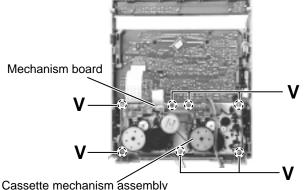


Fig.30

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<CD changer unit>

· Prior to performing the following procedure, remove the CD changer unit.

Removing the VCD board

(See Fig.31)

- 1. Disconnect the harness from connector PCON1 of the VCD board .
- 2. Remove the four screws W attaching the Sealed and VCD board.

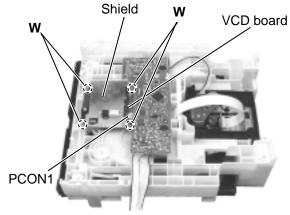


Fig.31

the CD servo board on the upper side of the CD Loading pulley gear marked c CD tray Fig.32 Tray stopper marked i CD tray Tray stopper marked i CD servo board SCW5 Fig.33 CD tray

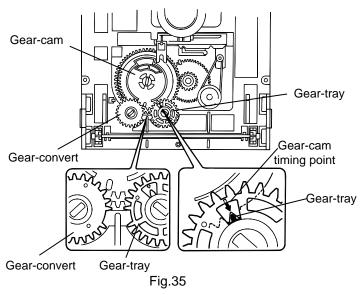


Removing the CD tray (See Fig.32 to 34)

- 1. Turn the black loading pulley gear marked c on the under side of the CD changer unit in the direction of the arrow and draw the CD tray toward the front until it stops.
- 2. Disconnect the card wire from connector SCW5 of changer unit.
- 3. Push down the two tray stoppers marked i and pull out the CD tray.

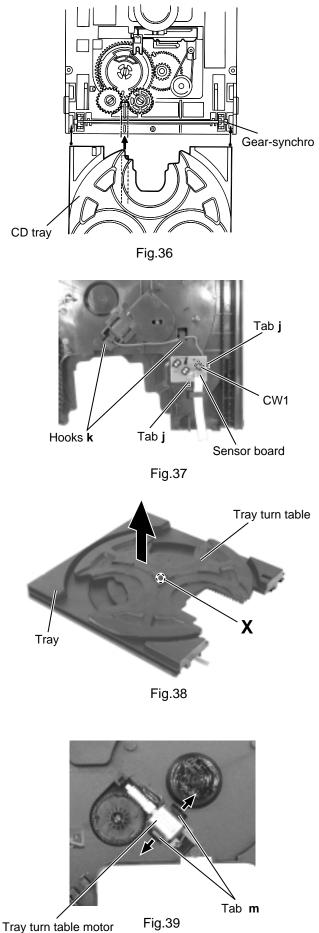
■ Reinstall the CD tray (See Fig.35 and 36)

- 1. Align the gear-cam with the gear-tray as shown fig.28, then mount the CD tray.
- 2. When assembling the CD tray, take extreme care not engage with gear synchro.



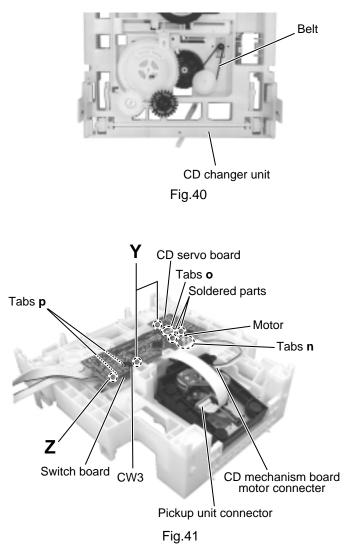
Removing the sensor board / the tray motor (See Fig.37 to 39)

- Prior to performing the following procedure, remove the CD tray.
- 1. Release the two tabs **j** attaching the sensor board on the under side of the CD tray.
- Disconnect the harness from connector CW1 on the sensor board and release the harness from the two hooks k. Remove the sensor board.
- 3. Remove the screw **X** attaching the tray turn table. Detach the tray turn table from the tray.
- 4. Pull outward the tab **m** attaching the tray turn table motor assembly on the upper side of the tray and detach the tray turn table motor assembly from the tray.



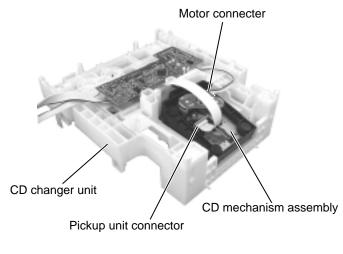
assembly

- Removing the belt, the CD servo board and the switch board (See Fig.40 and 41)
- Prior to performing the following procedure, remove the CD tray.
- 1. Detach the belt from the pulley on the upper side of the CD changer unit (Do not stain the belt with grease).
- 2. Disconnect the card wire from the pickup unit connector on the under side of the CD changer unit.
- 3. Disconnect the motor wire harness from connector on the CD mechanism board.
- 4. Remove the two screws Y attaching the CD servo board. First release the n side of the two tabs n and two tabs o attaching the CD servo board motor to raise the CD servo board slightly, then release the o side.
- % If the tabs **n** and **o** are hard to release, it is recommendable to unsolder the two soldered parts on the motor terminal of the CD servo board. Disconnect the terminal CW3 connected to the switch board and remove the CD servo board.
- 5. Remove the screw **Z** attaching the CD Changer unit and release the three tabs **p** attaching the switch board outward and detach the switch board.

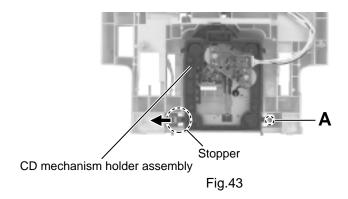


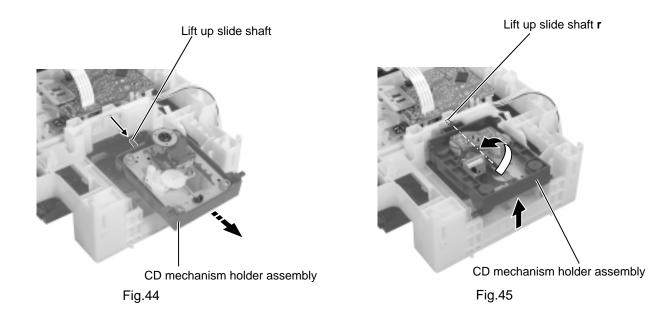
Removing the CD mechanism holder assembly (mechanism included) (See Fig.42 to 45)

- 1. Disconnect the harness from connector on the CD mechanism board in the CD mechanism assembly on the under side of the CD changer unit. Disconnect the card wire from the pickup unit connector.
- 2. Remove the screw **A** attaching the shaft on the right side of the CD mechanism holder assembly. Pull outward the stopper fixing the shaft on the left side and remove the CD mechanism holder assembly from behind in the direction of the arrow.
- 3. Turn the CD mechanism holder assembly half around the lift up slide shaft **r** of the CD mechanism holder assembly until the turn table is reversed, and pull out the CD mechanism holder assembly.









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<CD mechanism section>

 Removing the CD mechanism holder from the CD chassis to remove the CD mechanism. (Refer to "Removing the CD mechanism holder assembly" (Pag.2-11))

Removing the pickup unit.

- 1. Loosen the two screws A fixing the chassis.(Fig.1)
- Removing the feed gear stopper c on the bottom of the mechanism and pull out the gear. (Fig.1, Fig.3, Fig.4)
- 3. Pull out the shaft by opening the pickup shaft stopper outward to unlock.(Fig.1, Fig.2)
- 4. Removing the pickup unit.(Fig.1)

Removing the motor board.

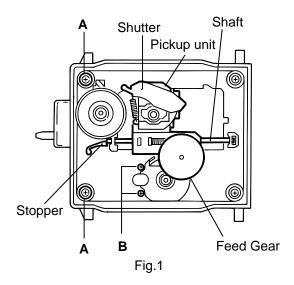
- 1. Unsolder the motor terminal on the motor board.(Fig.3)
- 2. Remove the motor board.(Fig.3)

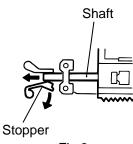
Removing the feed motor.

Remove the two motor fixing screws at **B** and removing the feed motor.(Fig.1, Fig.3)

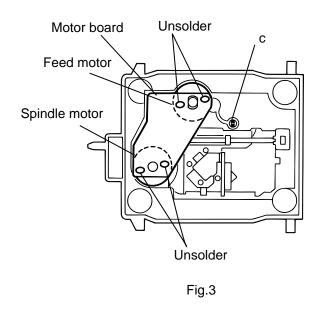
Removing the spindle motor.

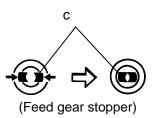
The spindle motor cannot be removed as a single unit. When removing the spindle motor, change the chassis and turntable together as aunit.(Fig.5)











Spindle motor

Fig.5

<Cassette mechanism section>

• Removing the record/playback mechanism.

■ Removing the R/P head.

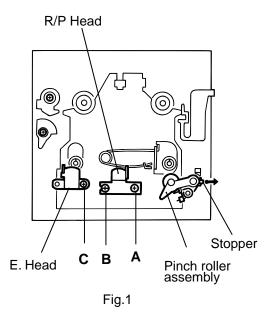
- 1. Remove the screw **A** on the right side of the R/P head.(Fig.1, Fig.2)
- 2. Remove the screw **B** on the left side of the R/P head.(Fig.1, Fig.2)

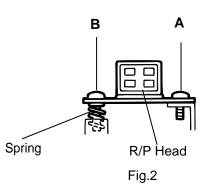
Remove the erase head.

Remove the screw **C** fixing the erase head.(Fig.1)

Removing the pinch roller.

- 1. Pull out the pinch roller by opening the pinch roller stopper outward to unlock .(Fig.3)
- 2. When reassembling the pinch roller, refer to fig. 4 to hook up the spring.





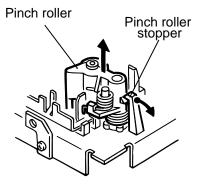
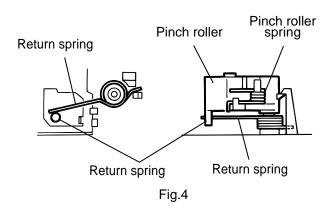


Fig.3



Removing the motor.

Removing the flywheel.

When reassembling the flywheel, be sure to use new washers as they cannot be reused.(Fig.8, Fig.9)

- Remove the two screws D fixing the motor. Be careful to grease's splash when the drive belt comes off.(Fig.5, Fig.6)
- 2. Unsolder the motor terminal.(Fig.5)

Removing the mechanism board.

- 1. Unsolder the four parts **a** on the solenoid coil terminal.(Fig.5)
- 2. Remove the two screws E fixing the board.(Fig.5)
- 3. Unhook the three parts **b** from the board.(Fig.5)
- 4. Remove the mechanism board.(Fig.5)

Remove the cut-washers at **c** and **d** from the capstan shaft, then remove the flywheel.

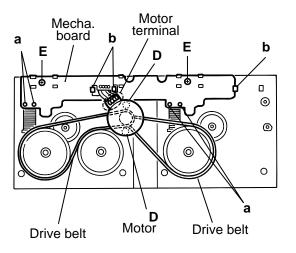
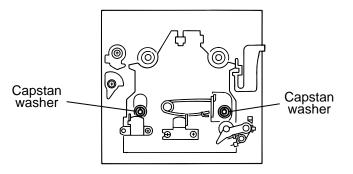
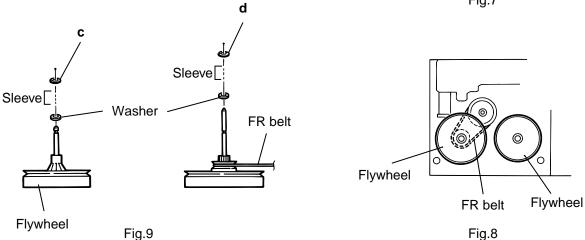


Fig.5

Motor Drive belt Fig.6



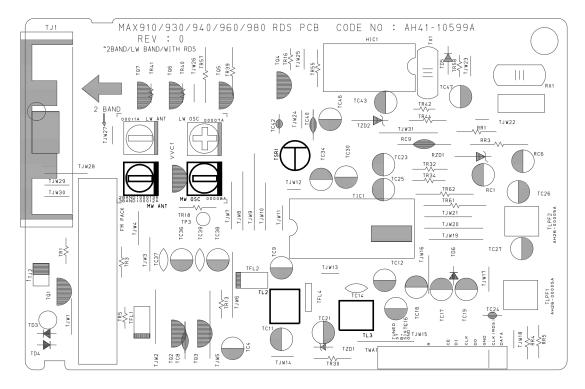




1-20

Adjustment method

Tuner



* Adjustment Location of Tuner PCB

ITEAM	AM(MW) OSC Adjustment	AM(MW) RF Adjustment
Received FREQ.	520~1720 KHz	590 KHz
Adjustment point	Non- Adjustment	MW-ANT
Output	1~7.0±0.5V	Maximum Output(Fig1-4)

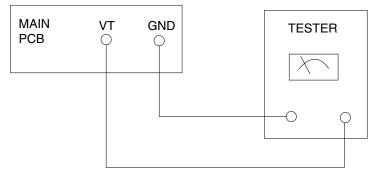


Fig 1-4 OSC Voltage

MX-J170V

FM THD Adjustment						
SSG FREQ.	98 MHz					
Adjustment point (TL3)	FM DETECTOR COIL					
Output	60 dB					
Minumum Distortion (0.3% below) (Figure 1-1)						

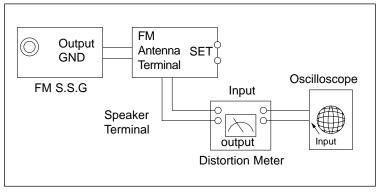


Figure1-1 IF CENTER and THD Adjustment

FM Search Level Adjustment					
SSG FREQ.	98 MHz				
Adjustment point (TSR1)	BEACON SENSITIVITY SEMI-VR(20K½)				
Output	28 dB(±2dB)				
Adjust TSR1 so is lighted (Figure	that "TUNED" of FL T = 1-2)				

*Adjust FM S.S.G level to 28dB

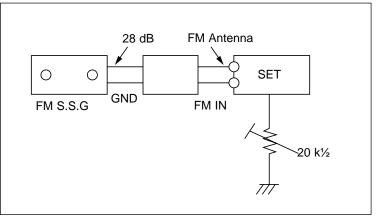


Figure1-2 FM Auto Search Level Adjustment

AM(MW) I.F Adjustment				
SSG FREQ.	450 kHz			
Frequency	520 kHz			
Adjustment point (TL2)	AM I.F COIL			
Maximum output (Figure 1-3)				

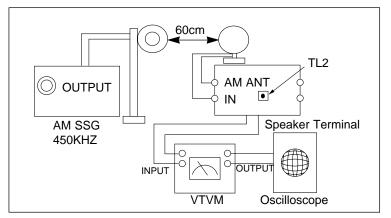


Figure1-3 AM I.F Adjustment

■ Cassette deck

1. To adjust tape speed

	-Notes]
.	1) Measuring tape: i) MTT -111 (or equivalent) (Tapes recorded with 3kHz) ii) MTT-5512 (or equivalent)	
	2) Connect the cassette deck to the frequency counter as in figure 1-5.	

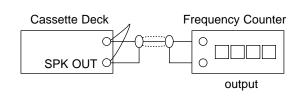
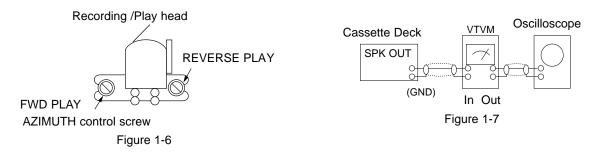


Figure 1-5

Step	Item	Pre-Setup Condition	Pre-Setup	To Adjust	Standard	Remark
1	NOR SPEED Control	OUT (connected to the frequency counter)	 Deck 1:MTT-111 Press PLAY SW button Deck 2:Same as above 	Turn UVR2 to left and right (FRONT PCB)	3KHz	±1% range



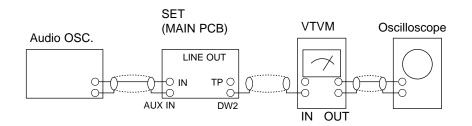


Figure 1-8

2. To adjust playback lebel/REC

-Notes

- Before the actual adjustment, clean the play/recording head.
- 2) Measuring tape :
 - i) MTT-114NA(or equivalent 12.5kHz AZIMUTH control)
 - ii) MTT-5512
- 3) The cassette deck is connections as shown in figure 1-7.

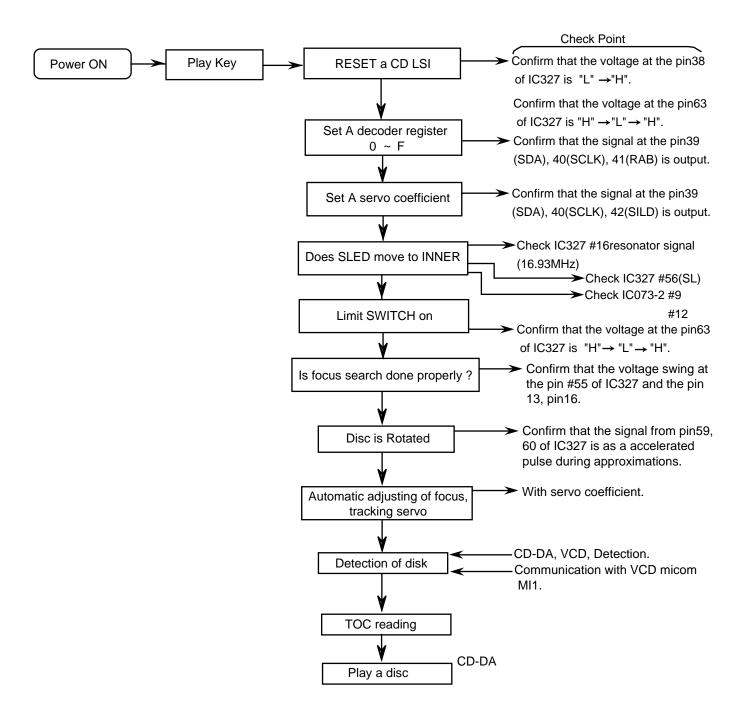
1 Adjust Deck 1 Play Level

Step	Item	Pre-Setup Condition	Pre-Setup	To Adjust	Standard	Remark
1	AZIMUTH	TP1 OUT (VTVM is connected to the scope)	After putting MTT - 114NA into Deck 1 - Press FWD PLAY button.	- Turn the control screw to as shown in Figure 1-6.	Max output and same phase (both channels)	After adjustment secure it with REGION LOCK.

2 Adjust Deck 2 Play Level/REC BIAS

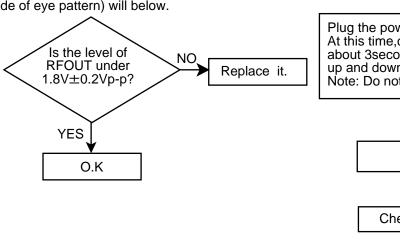
Step	Item	Pre-Setup Condition	Pre-Setup	To Adjust	Standard	Remark
1	AZIMUTH	TP1 OUT (VTVM is connected to the scope)	After putting MTT- 114NA into Deck 2 1)Press FWD PLAY button. 2)Press REV PLAY button.	- Turn the control screw to as shown in Figure 1-6.	Max output and same phase (both channels)	After adjustment secure it with REGION LOCK.
2	Recording Bias Voltage	Fig 1-8	After putting MT-T 5512 into Deck 2 1)Press REC PLAY button. 2)MAIN PCB DCW2, connectted to VTVM	Turn DVR1,DVR2 to the right and left	7V(±0.5V)	

Flow of functional operation until TOC read

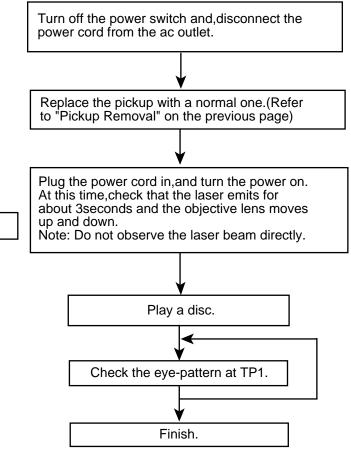


Maintenance of laser pickup

- Cleaning the pick up lens Before you replace the pick up, please try to clean the lens with a alcohol soaked cotton swab.
- (2) Life of the laser diodeWhen the life of the laser diode has expired, the following symptoms will appear.
 - 1. The level of RF output (EFM output:ampli tude of eye pattern) will below.



Replacement of laser pickup



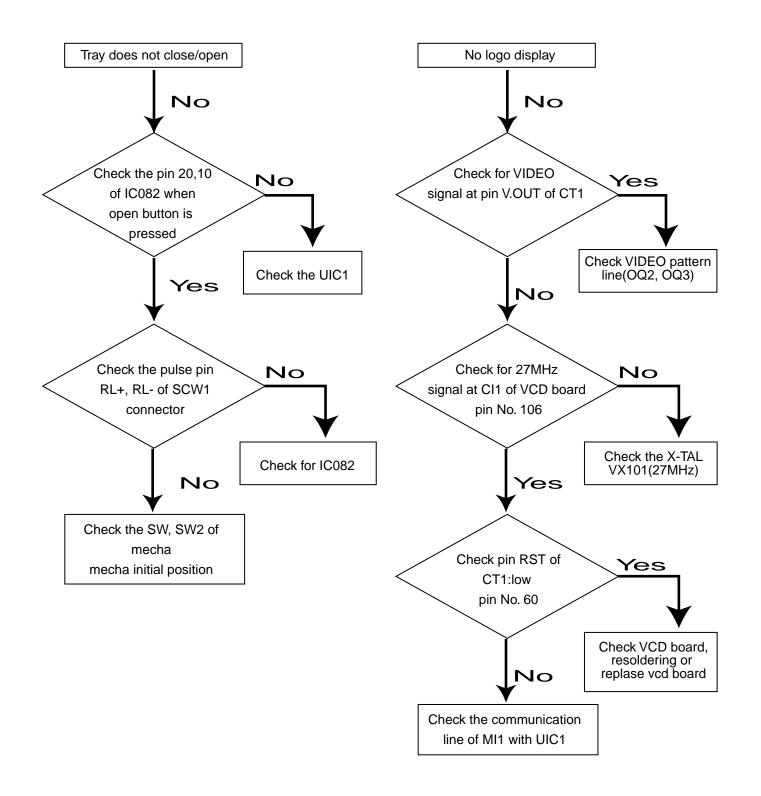
(3) Semi-fixed resistor on the APC PC board

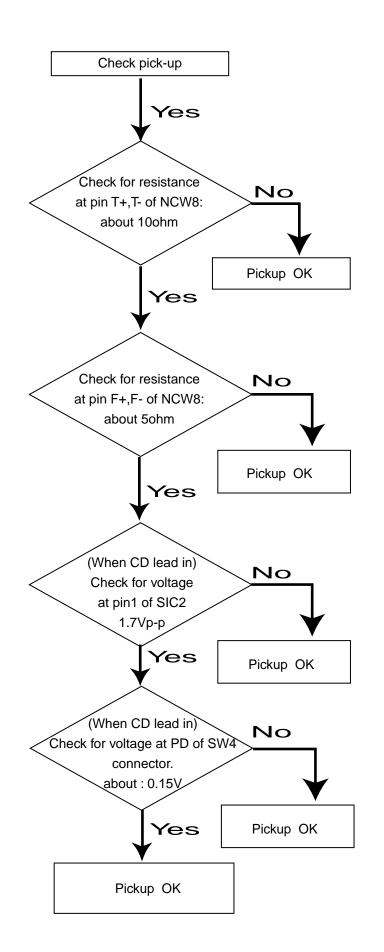
The semi-fixed resistor on the APC printed circuit board which is attached to the pickup is used to adjust the laser power. Since this adjustment should be performed to match the characteristics of the whole optical block, do not touch the semi-fixed resistor.

If the laser power is lower than the specified value, the laser diode is almost worn out, and the laser pickup should be replaced.

If the semi-fixed resistor is adjusted while the pickup is functioning normally, the laser pickup may be damaged due to excessive current.

Trouble shooting guide

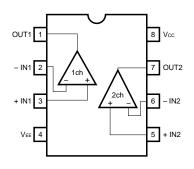




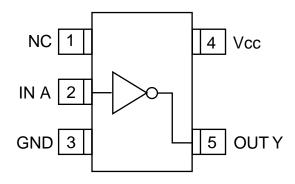
Description of major ICs

BA4560 (UIC1) / KA4558 (DIC2) : Dual OP AMP

1.Pin layout



TC7SU04F (C12) : Inverter



■ NJU3711M (UIC2) : 8-BIT Serial to parallel conveter

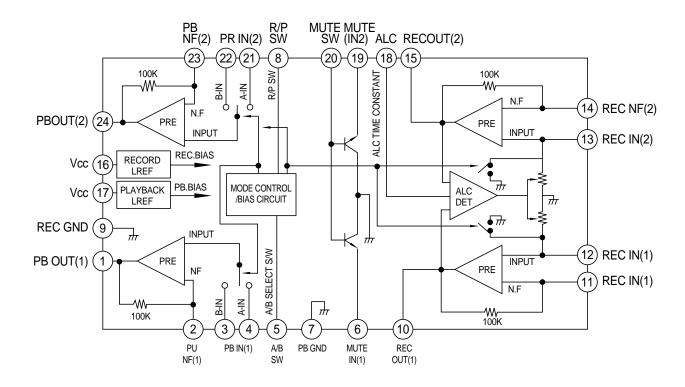
1. Pin layout

2. Pin function

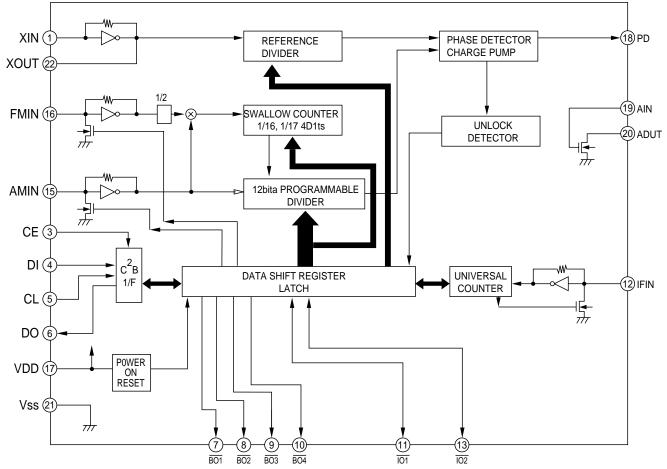
P3 1	14 V _{DD}
P4 2	13 P2
P5 3	12 P1
V _{SS} 4	11 CLR
P6 5	10 STB
P7 6	9 CLK
P8 7	8 DATA

Pin.No	Symbol	Function	
1	P3		
2	P4	Parallel converts darta output terminals	
3	P5		
4	V _{SS}	Ground	
5	P6		
6	P7	Parallel converts darta output terminals	
7	P8		
8	DATA	Serial data input termnal	
9	CLK	Clock signal input termnal	
10	STB	Strove signal input termnal	
11	CLR	Clear signal input termnal	
12	P1	Parallel converts darta output terminals Power supply terminal	
13	P2		
14	V _{DD}		

■ KA22291 (DIC1) : Cassette amp.

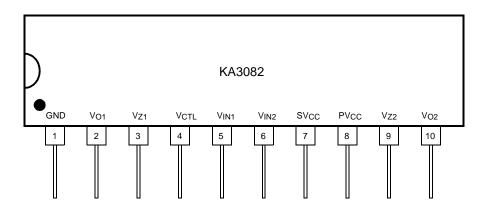


LC72131D (HIC1) : PLL



KA3082 (IC3082) : Bi-directional DC motor driver

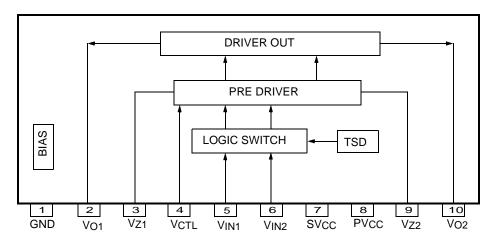
1.Pin layout



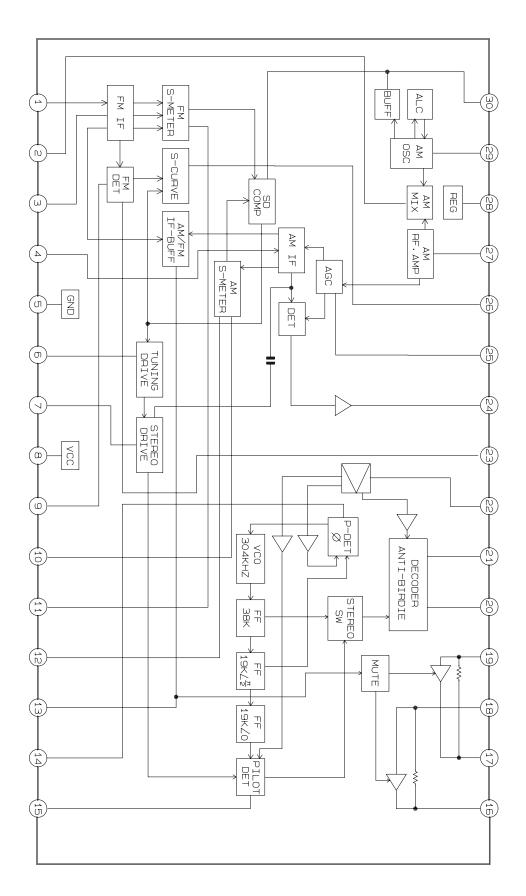
2.Pin function

Pin Nu mber	Pin Name	I/O	Pin Function Descriptio n
1	GND	-	Ground
2	VO1	0	Output 1
3	V _{Z1}	-	Phase compensation
4	VCTL	I	Motor speed control
5	VIN1	I	Input 1
6	VIN2	I	Input 2
7	SVCC	-	Supply voltage (Signal)
8	PVcc	-	Supply voltage (Power)
9	V _{Z2}	-	Phase compensation
10	VO2	0	Output 2

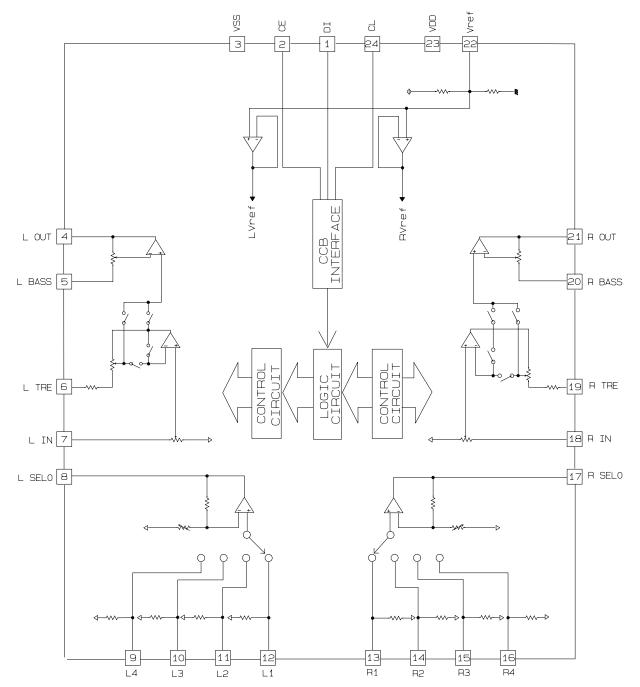
3.Block Diagram



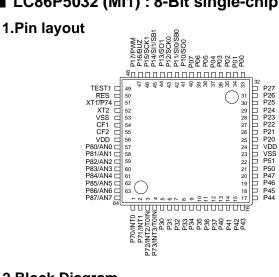
■ LA1837 (TIC1) : FM IF/DET AM RF/IF/DET

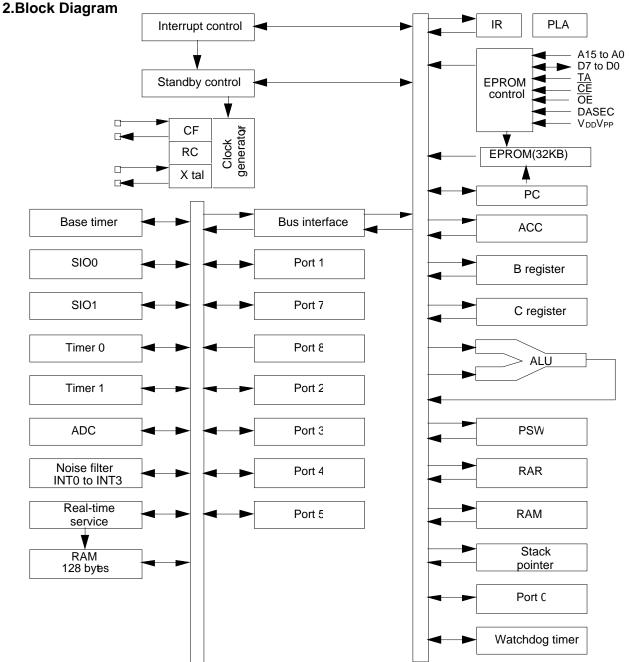


■ LC75341 (FIC1) : Function



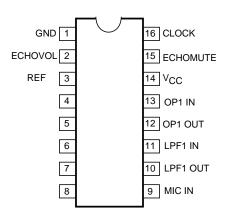
■ LC86P5032 (MI1) : 8-Bit single-chip microcontroller





■ M65855FP(EIC1) : Sound processor

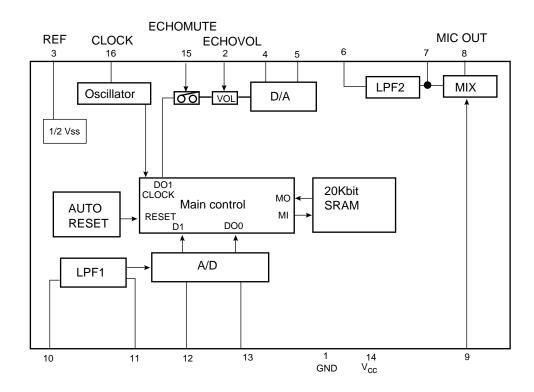
1. Pin layout



Pin No.	Symbol	DESCRIPTION	
1	GND		
2	ECHOVOL	Echo level control with external DC voltage	
3	REF	To connect 1/2 Vcc output and filter capacitor	
4	OP2 IN	Uses external C to from an D/A conversion	
5	OP2 OUT	integrator	
6	LPF2 IN	Uses external CR to from a low pass filter at the	
7	LPF2 OUT	input side	
8	MIC OUT	Mixing output echo output and microphone	
9	MIC IN	Microphone input	
10	LPF1 OUT	Uses external CR to from a low pass filter at the	
11	LPF1 IN	input side	
12	OP1 OUT	Uses external C to from an D/A conversion	
13	OP1 IN	integrator	
14	V _{CC}	Applies a voltage of 3.5V to 5.5V(Rated5V)	
15	ECHOMUTE	Echo mute control and clock stop control with external DC voltage	
16	CLOCK	Controls a built -in clock generation circuit with external R	

2. Pin function

3. Block diagram.



■ NJU3711M (UIC2) : 8-BIT Serial to parallel converter

1. Pin layout

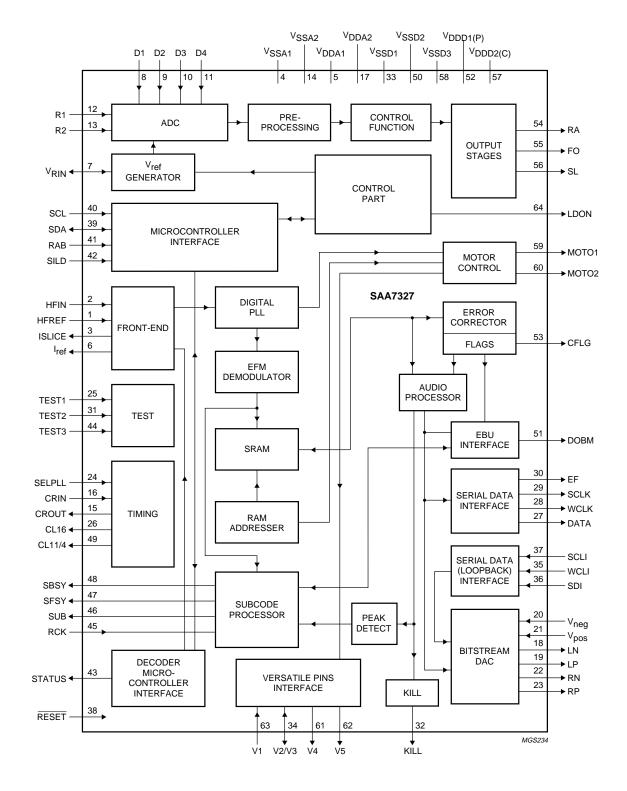
2. Pin function

P3 1	14 V _{DD}
P4 2	13 P2
P5 3	12 P1
VSS 4	11 CLR
P6 5	10 STB
P7 6	9 CLK
P8 7	8 DATA
1	

Pin.No	Symbol	Function	
1	P3		
2	P4	Parallel converts data output terminals	
3	P5		
4	V _{SS}	Ground	
5	P6		
6	P7	Parallel converts data output terminals	
7	P8		
8	DATA	Serial data input termnal	
9	CLK	Clock signal input termnal	
10	STB	Strove signal input termnal	
11	CLR	Clear signal input termnal	
12	P1	Parallel converts data output terminals Power supply terminal	
13	P2		
14	V _{DD}		

SAA7327 (IC327) :Digital servo processor

1. Block diagram



2. Pin function

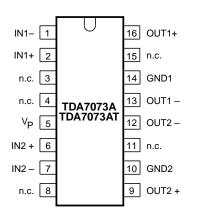
1HFREFcomparator common mode input2HFINcomparator signal input3ISLICEcurrent feedback output from data slicer $4^{(1)}$ V_{SSA1} analog ground 1 $5^{(1)}$ V_{DDA1} analog supply voltage 16 I_{ref} reference current output7 V_{RIN} reference voltage for servo ADCs8D1unipolar current input 1 (central diode signal input)9D2unipolar current input 2 (central diode signal input)10D3unipolar current input 3 (central diode signal input)11D4unipolar current input 2 (central diode signal input)12R1unipolar current input 2 (satellite diode signal input)13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹¹⁾ V_{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator output17 ⁽¹¹⁾ V_{DDA2} analog supply voltage 218LNDAC left channel differential negative output20 V_{neg} DAC negative reference input21 V_{pos} DAC negative reference input22RNDAC right channel differential positive output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output (3-state)<		Symbol	Function	
3ISLICEcurrent feedback output from data slicer $4^{(1)}$ V_{SSA1} analog ground 1 $5^{(1)}$ V_{DDA1} analog supply voltage 16 I_{ref} reference current output7 V_{RIN} reference voltage for servo ADCs8D1unipolar current input 1 (central diode signal input)9D2unipolar current input 2 (central diode signal input)10D3unipolar current input 3 (central diode signal input)11D4unipolar current input 4 (central diode signal input)12R1unipolar current input 4 (central diode signal input)13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹⁾ V_{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator output17 ⁽¹⁾ V_{DDA2} analog supply voltage 218LNDAC left channel differential negative output20 V_{neg} DAC negative reference input21 V_{pos} DAC positive reference input22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	1	HFREF	comparator common mode input	
$4^{(1)}$ V_{SSA1} analog ground 1 $5^{(1)}$ V_{DDA1} analog supply voltage 1 6 I_{ref} reference current output7 V_{RIN} reference voltage for servo ADCs8D1unipolar current input 1 (central diode signal input)9D2unipolar current input 2 (central diode signal input)10D3unipolar current input 3 (central diode signal input)11D4unipolar current input 4 (central diode signal input)12R1unipolar current input 1 (satellite diode signal input)13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹⁾ V_{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator input17 ⁽¹⁾ V_{DDA2} analog supply voltage 218LNDAC left channel differential negative output20 V_{neg} DAC negative reference input21 V_{pos} DAC right channel differential negative output22RNDAC right channel differential negative output23RPDAC right channel differential negative output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	2	HFIN	comparator signal input	
$5^{(1)}$ VDDA1 PDA1analog supply voltage 16 I_{ref} reference current output7 V_{RIN} reference current output9D2unipolar current input 1 (central diode signal input)9D2unipolar current input 2 (central diode signal input)10D3unipolar current input 3 (central diode signal input)11D4unipolar current input 4 (central diode signal input)12R1unipolar current input 1 (satellite diode signal input)13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹⁾ V_{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator output17 ⁽¹⁾ V_{DDA2} analog supply voltage 218LNDAC left channel differential negative output20 V_{neg} DAC negative reference input21 V_{pos} DAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	3	ISLICE	current feedback output from data slicer	
6Irefreference current output7 V_{RIN} reference voltage for servo ADCs8D1unipolar current input 1 (central diode signal input)9D2unipolar current input 2 (central diode signal input)10D3unipolar current input 3 (central diode signal input)11D4unipolar current input 4 (central diode signal input)12R1unipolar current input 1 (satellite diode signal input)13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹⁾ V_{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator output17 ⁽¹⁾ V_{DDA2} analog supply voltage 218LNDAC left channel differential negative output20 V_{neg} DAC negative reference input21 V_{pos} DAC roght channel differential negative output22RNDAC right channel differential negative output23RPDAC right channel differential negative output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	4 ⁽¹⁾	V _{SSA1}	analog ground 1	
7 V_{RIN} reference voltage for servo ADCs8D1unipolar current input 1 (central diode signal input)9D2unipolar current input 2 (central diode signal input)10D3unipolar current input 3 (central diode signal input)11D4unipolar current input 4 (central diode signal input)12R1unipolar current input 1 (satellite diode signal input)13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹⁾ V_{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator input17 ⁽¹⁾ V_{DDA2} analog supply voltage 218LNDAC left channel differential negative output20 V_{neg} DAC negative reference input21 V_{pos} DAC positive reference input22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)	5 ⁽¹⁾	V _{DDA1}	analog supply voltage 1	
8D1unipolar current input 1 (central diode signal input)9D2unipolar current input 2 (central diode signal input)10D3unipolar current input 3 (central diode signal input)11D4unipolar current input 4 (central diode signal input)12R1unipolar current input 1 (satellite diode signal input)13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹⁾ V_{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator input17 ⁽¹⁾ V_{DDA2} analog supply voltage 218LNDAC left channel differential negative output20 V_{neg} DAC negative reference input21 V_{pos} DAC rogitive reference input22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	6	I _{ref}	reference current output	
9D2unipolar current input 2 (central diode signal input)10D3unipolar current input 3 (central diode signal input)11D4unipolar current input 4 (central diode signal input)12R1unipolar current input 1 (satellite diode signal input)13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹⁾ V _{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator output17 ⁽¹⁾ V _{DDA2} analog supply voltage 218LNDAC left channel differential negative output19LPDAC left channel differential positive output20V _{neg} DAC negative reference input21V _{pos} DAC right channel differential negative output23RPDAC right channel differential negative output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	7	V _{RIN}	reference voltage for servo ADCs	
10D3unipolar current input 3 (central diode signal input)11D4unipolar current input 4 (central diode signal input)12R1unipolar current input 1 (satellite diode signal input)13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹⁾ V _{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator input17 ⁽¹⁾ V _{DDA2} analog supply voltage 218LNDAC left channel differential negative output19LPDAC left channel differential positive output20V _{neg} DAC negative reference input21V _{pos} DAC positive reference input23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	8	D1	unipolar current input 1 (central diode signal input)	
11D4unipolar current input 4 (central diode signal input)12R1unipolar current input 1 (satellite diode signal input)13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹⁾ V _{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator input17 ⁽¹⁾ V _{DDA2} analog supply voltage 218LNDAC left channel differential negative output19LPDAC left channel differential positive output20V _{neg} DAC negative reference input21V _{pos} DAC positive reference input23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	9	D2	unipolar current input 2 (central diode signal input)	
12R1unipolar current input 1 (satellite diode signal input)13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹⁾ V _{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator input17 ⁽¹⁾ V _{DDA2} analog supply voltage 218LNDAC left channel differential negative output19LPDAC left channel differential positive output20V _{neg} DAC negative reference input21V _{pos} DAC positive reference input22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	10	D3	unipolar current input 3 (central diode signal input)	
13R2unipolar current input 2 (satellite diode signal input)14 ⁽¹⁾ V _{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator input17 ⁽¹⁾ V _{DDA2} analog supply voltage 218LNDAC left channel differential negative output19LPDAC left channel differential positive output20V _{neg} DAC negative reference input21V _{pos} DAC positive reference input22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	11	D4	unipolar current input 4 (central diode signal input)	
14(1)V _{SSA2} analog ground 215CROUTcrystal/resonator output16CRINcrystal/resonator input17(1)V _{DDA2} analog supply voltage 218LNDAC left channel differential negative output19LPDAC left channel differential positive output20V _{neg} DAC negative reference input21V _{pos} DAC positive reference input22RNDAC right channel differential positive output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	12	R1	unipolar current input 1 (satellite diode signal input)	
15CROUTcrystal/resonator output16CRINcrystal/resonator input17 ⁽¹⁾ V _{DDA2} analog supply voltage 218LNDAC left channel differential negative output19LPDAC left channel differential positive output20V _{neg} DAC negative reference input21V _{pos} DAC positive reference input22RNDAC right channel differential positive output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	13	R2	unipolar current input 2 (satellite diode signal input)	
16CRINcrystal/resonator input17(1)V _{DDA2} analog supply voltage 218LNDAC left channel differential negative output19LPDAC left channel differential positive output20V _{neg} DAC negative reference input21V _{pos} DAC positive reference input22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	14 ⁽¹⁾	V _{SSA2}	analog ground 2	
17 ⁽¹⁾ V _{DDA2} analog supply voltage 218LNDAC left channel differential negative output19LPDAC left channel differential positive output20V _{neg} DAC negative reference input21V _{pos} DAC positive reference input22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	15	CROUT	crystal/resonator output	
18LNDAC left channel differential negative output19LPDAC left channel differential positive output20VnegDAC negative reference input21VposDAC positive reference input22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	16	CRIN	crystal/resonator input	
19LPDAC left channel differential positive output20VnegDAC negative reference input21VposDAC positive reference input22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	17 ⁽¹⁾	V _{DDA2}	analog supply voltage 2	
20VnegDAC negative reference input21VposDAC positive reference input22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	18	LN	DAC left channel differential negative output	
21VposDAC positive reference input22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	19	LP	DAC left channel differential positive output	
22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	20	V _{neg}	DAC negative reference input	
22RNDAC right channel differential negative output23RPDAC right channel differential positive output24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	21	V _{pos}	DAC positive reference input	
24SELPLLselects whether internal clock multiplier PLL is used25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	22		DAC right channel differential negative output	
25TEST1test control input 1 (this pin should be tied LOW)26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	23	RP	DAC right channel differential positive output	
26CL1616.9344 MHz system clock output27DATAserial d4(1) data output (3-state)28WCLKword clock output (3-state)	24	SELPLL	selects whether internal clock multiplier PLL is used	
27 DATA serial d4(1) data output (3-state) 28 WCLK word clock output (3-state)	25	TEST1	test control input 1 (this pin should be tied LOW)	
28 WCLK word clock output (3-state)	26	CL16	16.9344 MHz system clock output	
	27	DATA	serial d4(1) data output (3-state)	
29 SCLK serial bit clock output (3-state)	28	WCLK	word clock output (3-state)	
	29	SCLK	serial bit clock output (3-state)	
30 EF C2 error ßag output (3-state)	30	EF	C2 error ßag output (3-state)	
31 TEST2 test control input 2 (this pin should be tied LOW)	31	TEST2	test control input 2 (this pin should be tied LOW)	
32 KILL kill output (programmable; open-drain)	32	KILL	kill output (programmable; open-drain)	
33 ⁽¹⁾ V _{SSD1} digital ground 1	33(1)	V _{SSD1}	digital ground 1	
34 V2/V3 versatile I/O: versatile input 2 or versatile output 3 (open-drain)	34	V2/V3	versatile I/O: versatile input 2 or versatile output 3 (open-drain)	
35 WCLI word clock input (for data loopback to DAC)	35	WCLI	word clock input (for data loopback to DAC)	
36 SDI serial data input (for data loopback to DAC)	36	SDI	serial data input (for data loopback to DAC)	
37 SCLI serial bit clock input (for data loopback to DAC)	37	SCLI	serial bit clock input (for data loopback to DAC)	
38 RESET power-on reset input (active LOW)	38	RESET	power-on reset input (active LOW)	
39 SDA microcontroller interface data I/O line (I ² C-bus; open-drain output)	39	SDA	microcontroller interface data I/O line (I ² C-bus; open-drain output)	
40 SCL microcontroller interface clock line input (I ² C-bus)	40	SCL	microcontroller interface clock line input (I ² C-bus)	

2. Pin function(2/2)

Pin No.	Symbol	Function
41	RAB	microcontroller interface R/W and load control line input (4-wire bus mode)
42	SILD	microcontroller interface R/W and load control line input (4-wire bus mode)
43	STATUS	servo interrupt request line/decoder status register output (open-drain)
44	TEST3	test control input 3 (this pin should be tied LOW)
45	RCK	subcode clock input
46	SUB	P-to-W subcode bits output (3-state)
47	SFSY	subcode frame sync output (3-state)
48	SBSY	subcode block sync output (3-state)
49	CL11/4	11.2896 or 4.2336 MHz (for microcontroller) clock output
50 ⁽¹⁾	V _{SSD2}	digital ground 2
51	DOBM	bi-phase mark output (externally buffered; 3-state)
52(1)	V _{DDD1(P)}	digital supply voltage 1 for periphery
53	CFLG	correction ßag output (open-drain)
54	RA	radial actuator output
55	FO	focus actuator output
56	SL	sledge control output
57 ⁽¹⁾	V _{DDD2(C)}	digital supply voltage 2 for core
58(1)	V _{SSD3}	digital ground 3
59	MOTO1	motor output 1; versatile (3-state)
60	MOTO2	motor output 2; versatile (3-state)
61	V4	versatile output 4
62	V5	versatile output 5
63	V1	versatile input 1
64	LDON	laser drive on output (open-drain)

TDA7073A(IC805) : Dual BTL power driver

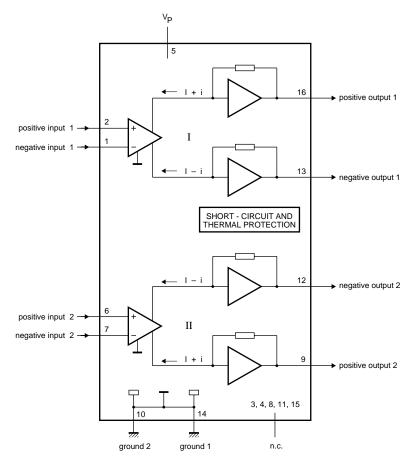
1. Pin layout



2. Pin function

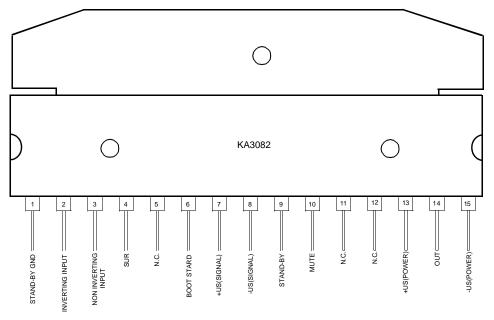
Pin No.	Symbol	Function
1	IN1-	negative input 1
2	IN1+	positive input 1
3	n.c.	not connected
4	n.c.	not connected
5	V _P	positive supply voltage
6	IN2+	positive input 2
7	IN2-	negative input 2
8	n.c.	not connected
9	OUT2+	positive output 2
10	GND2	ground 2
11	n.c.	not connected
12	OUT2+	negative output 2
13	OUT1-	negative output 1
14	GND1	ground 1
15	n.c.	not connected
16	OUT1+	positive output 1

3. Block diagram

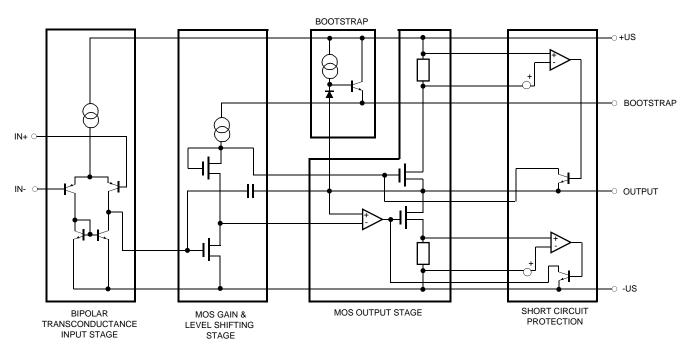


■ TDA7295 (AIC1, 2) : Audio amp.

1.Pin layout



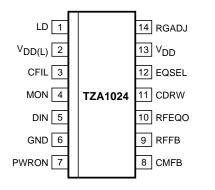
2.Block Diagram



■ TZA1024 (IC024) : Data ampliber and laser supply

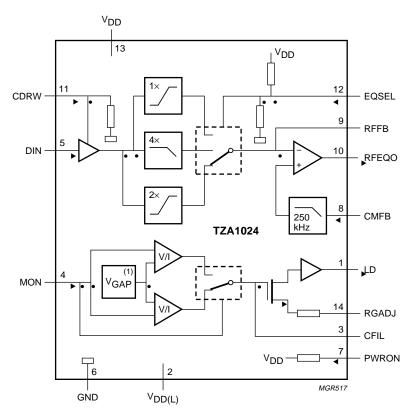
1. Pin Layout

2. Pin function



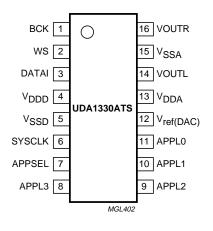
PIN.No	SYMBOL	Function
1	LD	current output to laser diode
2	V _{DD(L)}	laser supply voltage
3	CFIL	external Plter capacitor
4	MON	laser monitor diode input
5	DIN	central diode input
6	GND	ground
7	PWRON	power-on select input
8	CMFB	common mode feedback voltage input
9	RFFB	external RF feedback resistor
10	RFEQO	RF ampliÞer output
1	CDRW	gain select input for CD-A/V , CD-R/W
12	EQSEL	equalizer/speed select input (n = 1, 2 or 4)
13	V _{DD}	supply voltage
14	RGADJ	external laser supply gain adjust resistor

3. Block diagram



UDA1330AT (AI1) : Stereo filter DAC

1. Pin layout



2. Pin function

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATAI	3	data input
V _{DDD}	4	digital supply voltage
V _{SSD}	5	digital ground
SYSCLK	6	system clock input: $256f_s$, $384f_s$ and $512f_s$
APPSEL	7	application mode select input
APPL3	8	application input 3
APPL2	9	application input 2
APPL1	10	application input 1
APPL0	11	application input 0
V _{ref(DAC)}	12	DAC reference voltage
V _{DDA}	13	analog supply voltage for DAC
VOUTL	14	left channel output
V _{SSA}	15	analog ground
VOUTR	16	right channel output

3. Block diagram.

